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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,975	08/13/2001	Scott Brad Herner	10519-57	7752

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,975	HERNER ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Reopening of Prosecution

1. In view of the Appeal Brief filed on January 21, 2004, PROSECUTION IS HEREBY RE-OPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Commentary

2. Claims 1 – 4, and 7 contain limitations related to a product produced by process. "The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). MPEP 2113.

3. In Claim 1, the limitations,

"*a second semiconductor region overlying the first semiconductor region , said*

semiconductor region comprising silicon and characterized by a dopant concentration less than 1 x 10^(19)/cm(3) and a thickness, t1"

"a layer comprising titanium directly overlying the second semiconductor region, said layer characterized by a line width no greater than 0.3um and a thickness t2, wherein t1 > 1.2 t2,"

" t1/t2 being sufficiently small that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region,"

"t1/t2 being sufficiently large that, when the layer is reacted with the second semiconductor region to form titanium disilicide,"

have not been given patentable weight.

4. Limitations of Claims 2 – 4 have not been given patentable weight.

5. In Claim 7, the limitation, "*wherein the set of titanium silicide conductors is formed, in part, by a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than 1 x 10^(18)/cm(3),"* has not been given patentable weight.

6. All of the limitations listed refer to the state of an intermediate product, and not to the final state of the product, since the elements are not found in the final product.

Claim Rejections – 35 U.S.C. 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 – 7 are rejected under 35 U.S.C. 103(a) over Hu et al. (US2002/0045342 A1) in view of Spinelli et al. ("An improved Formula for the Determination of the Polysilicon Doping," IEEE Electron Device Letters, Vol. 22, No. 6, (June, 2001), pp.281 – 283) and Nakayama et al. ("Excellent Process Control Technology for Highly Manufacturable and High Performance 0.18um CMOS LSIs," Digest of Tech. Papers, Symp. on VLSI Technology (1998), pp. 146 – 147).

8. Regarding Claims 1 – 4, Hu et al. disclose a semiconductor structure comprising a doped first silicon layer (314) (Figure 3H) and a titanium silicide layer (332), wherein the final product is the titanium silicide layer.

Hu et al. do not explicitly disclose the doping concentration of the first semiconductor region, but typical doping of silicon over gate oxides is greater than 10^(19)/cm(3). (See for example, Spinelli et al., page 282, Figure 2). It would have been obvious to one of

ordinary skill in the art at the time of the invention to combine Spinelli et al. and Hu et al. to provide doping (> 10^(19)/cm(3)) for stable gate oxide interface electrical properties (p.3, para. [0029]) .

Further, Hu et al. do not disclose the sheet resistance after forming the titanium silicide. Nakayama et al. disclose (Figure 5) for structures of width less than or equal to 0.25um, titanium silicide conductor sheet resistances below 2.0 ohms/square. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the procedures of Nakayama et al. with Hu et al. and Spinelli et al. to obtain structures of low sheet resistance, reducing switching time.

9. Regarding Claim 5, Hu et al. do not disclose doped first silicon layers of concentration greater than 10^(20)/cm(3). As discussed earlier, this range of doping is routine in the art for gate structures (Spinelli et al. Figure 2, and p. 283). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Spinelli et al. with Hu et al. and Nakayama et al. to improve switching.

10. Regarding Claim 6, Hu et al. disclose that the semiconductor region is a "doped" layer (para. [0056], p.6) and it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize boron doping (p. 2, para. [0023] through top lines, p.3 left side)) to provide good interfacial properties adjacent to a gate oxide layer.

10. Regarding Claim 7, Hu et al. disclose a semiconductor structure comprising a doped silicon layer (314) (Figure 3C) with titanium silicide conductors (332) of width no greater than 0.3um (para. [0034], p. 3) on the first semiconductor region. Hu et al. do not disclose sheet resistances less than 3 ohms/square on the silicide conductors. Nakayama et al. disclose (Figure 5) for structures of width less than or equal to 0.25um, titanium silicide conductor sheet resistances below 2.0 ohms/square. It would have been obvious to one of ordinary skill in the art at the

time of the invention to combine the procedures of Nakayama et al. with Hu et al. and Spinelli et al. to obtain structures of low sheet resistance, reducing switching time. Further, Hu et al. do not disclose doped silicon layers of concentration greater than 10^(20)/cm(3). As discussed earlier, this range of doping is routine in the art for gate structures (Spinelli et al. Figure 2, and p. 283). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Spinelli et al. with Hu et al. and Nakayama et al. to improve switching.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. in view of Spinelli et al., and Nakayama et al., as applied to Claims 1 – 7, and further in view of Tsukude et al. ("A 256Mb DRAM," Advance Magazine, Mitsubishi Electric (June, 1996) Vol. 75, pp. 5 – 8).

Hu et al. disclose ([0002] through [0004]) that the structure comprises a memory array With stacked layers in the word line. However, it would be obvious that other circuit ele-

ments are required to complete an integrated circuit, including bit lines, associated passive components and interconnections, all of which would be stacked in a vertical 3D sequence because of limited area. It has been well established in the art (See Tsukude et al., p. 5) that DRAM devices with a 0.25um design rule effectively utilize a stacked memory cell architecture. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Tsukunde et al. with Hu et al. and Spinelli et al. to produce a complete working device.

Conclusions

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
April 16, 2004

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